HARRIS SEMICONDUCTOR

HSP50110

ADVANCE INFORMATION

February 1994

Digital Quadrature Tuner

Features

- 10 bit Real or Complex Inputs
- Frequency Selectivity <0.014Hz
- Data Rates to 60MSPS
- Third Order Cascaded-Integrator-Comb (CIC) Filter configurable as Integrate and Dump Filter (First Order CIC) or Bypassable
- Decimation from 1-4096, or Set by Resampling NCO used for Bit Synchronization
- Error Detection for External IF AGC Loop
- Internal AGC Loop for Output Level Stability
- Bi-Directional 8-Bit Microprocessor Interface
- Parallel or Serial Output Data Formats

Applications

- Phase and Frequency Modulation
- VSAT, INMARSAT Systems

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP50110JC-60	0°C to +70°C	84 Lead PLCC

Description

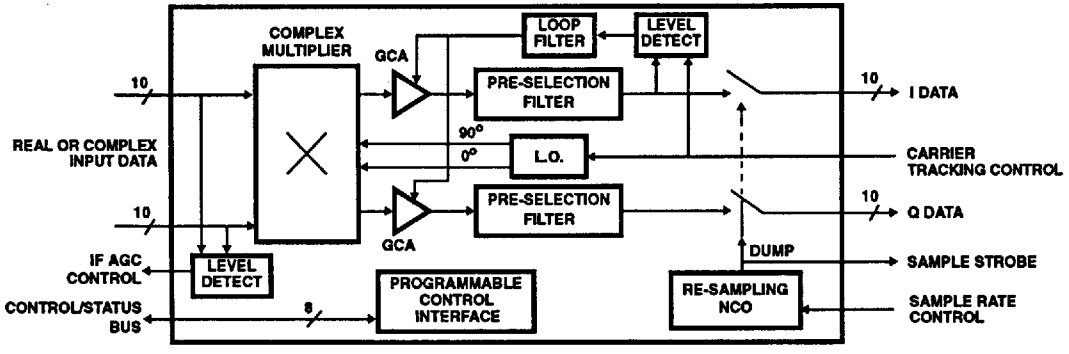
The Digital Quadrature Tuner (DQT) provides many of the functions needed for digital demodulation. These functions include carrier L.O. generation, symbol clock generation, preselection filtering, baseband AGC, and IF AGC error detection. The DQT facilitates many different digital implementations of demodulator tracking loops, which allows this chip to handle multiple modes and/or data rates simply by loading a new set of control words.

The DQT accepts digitized signals in either a real or complex representation. The digitized band of interest is shifted to DC through a complex multiplication by an internally generated L.O. The quadrature LO is generated by a numerically controlled oscillator (NCO) with a tuning resolution of approximately 14MHz at a clock rate of 60MHz and a spurious free dynamic range of 60dB. For added flexibility, a control interface is provided for real time phase and frequency updates.

The output of the complex multiplier is gain corrected and feed into identical preselection filters on both the real and imaginary processing legs. Each preselection filter is comprised of a decimating low pass filter followed by a compensation filter. The decimating low pass filter is a 3 stage cascade-integrator-comb (CIC) filter. The CIC filter can be bypassed, configured as an integrate and dump filter with a sin(X)/X response, or a third order filter with a $(\sin(X)/X)^3$ response. The decimation of the CIC filter stage may be fixed from 1-4096, or it may be controlled by a re-sampling NCO used for bit synchronization. The compensation filter is user selectable for flattening the $(\sin(X)/X)^N$ response of the CIC. These onboard filters may be bypassed if custom external filtering is required.

Level detectors are provided to generate error signals for external/internal AGC loops. The DQT output is provided in either serial or parallel formats to support interfacing with a variety DSP processors or digital filter components. This device is configurable over a general purpose 8-bit parallel bi-directional microprocessor control bus.

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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